

WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:
a package having a plurality of interface pins; and
a plurality of integrated circuit devices mounted
inside the package, wherein:

5 each integrated circuit device has a
plurality of interface ports, at least one
interface port being connected to another one of
the plurality of integrated circuit devices;

10 at least one of said integrated circuit
devices has an interface port connected to an
interface pin; and

at least one of said integrated circuit
devices is packaged in a chip scale package.

2. The integrated circuit device defined in claim 1
wherein some of said integrated circuit devices are not in
chip scale packages and have been tested at their full
operational speed.

3. The integrated circuit device defined in claim 1
wherein at least one of said integrated circuit devices is
a network processor and at least one of said other devices
is a memory device.

4. The integrated circuit device defined in claim 1
wherein the interconnections between said devices have
different impedances.

5. An integrated circuit interconnect module for
reducing interconnections between fully tested integrated
circuit chips comprising a support substrate having mounted
thereon at least one primary integrated circuit device chip
5 and a plurality of interacting peripheral integrated chip
devices, said interconnect module including a plurality of
interface pins, each integrated circuit device having a
plurality of interface ports, at least one of which is
connected to another one of said plurality of integrated
10 circuit devices, at least one of said integrated circuit
devices having an interface port connected to an interface
pin whereby the majority of nodes on said peripheral
devices are adapted to interface with nodes of one or more
primary IC devices in such a way as to condense the number
15 of nets so that the total number of nodes connected to
external pins is minimized.